a circuit partitioner for synthesizing from a user circuit a first circuit partition and a second circuit partition; and

a configurer configuring (a) said first circuit partition in said first programmable logic device and said second circuit partition in said second programmable logic device, and (b) said cross point switch for routing said data stream between said first input/output pin and said second input/output pin.

8. (Amended) A method, comprising:

synthesizing from a user circuit a first circuit partition and a second circuit partition;

configuring said first circuit partition in a first programmable logic device and said second circuit partition in a second programmable logic device, said configuring providing output signals of said first circuit partition designated for said second circuit partition as output signals of the first programmable logic device, and providing input signals of said second circuit partition as input signals to said second programmable logic device;

serializing said output signals of said first programmable logic device to provide a serialized data stream;

configuring a cross point switch to route said serialized data stream from a first input/output pin of said cross point switch onto a second input/output pin of said cross point switch; and

deserializing said data stream from said cross point switch as said input signals of said second programmable logic device.

14. (Amended) An emulator circuit, comprising:

a first programmable logic device and a second programmable logic device, wherein (a) said first programmable logic device includes a serializer, configurable to receive output signals from a user circuit configurable on said first programmable logic device and to serialize said output signals to provide a data stream on an input/output pin of said programmable logic device, and (b) said second programmable logic device includes a deserializer configurable to receive said serialized data stream from an input/output pin of said second programmable logic device and to deserialize said data

stream as input signals to a user circuit configurable on said second programmable logic device; and

a cross point switch receiving said data stream from said input/output pin of said first programmable logic device at a first input/output pin of said cross point switch and configurable to route said data stream onto a second input/output pin of said cross point switch coupled to said input/output pin of said second programmable logic device.

15. (Amended) An emulator including the emulator circuit of Claim 14, said emulator comprising:

a circuit partitioner for synthesizing from a user circuit a first circuit partition and a second circuit partition; and

a configurer configuring (a) said first circuit partition in said first programmable logic device and said second circuit partition in said second programmable logic device, and (b) said cross point switch for routing said data stream between said first input/output pin and said second input/output pin.

20. (Amended) A method, comprising:

synthesizing from a user circuit a first circuit partition and a second circuit partition;

configuring said first circuit partition in a first programmable logic device and said second circuit partition in a second programmable logic device, said configuring includes providing a serializer in said first programmable logic device for serializing output signals of said first circuit partition designated for said second circuit partition as a serialized data stream provided on an input/output pin of said first programmable logic device, and providing a deserializer in said second programmable logic device to deserialize said serialized data stream received at an input/output pin of said second programmable logic device as input signals of said second circuit partition; and

configuring a cross point switch to route said serialized data stream from a first input/output pin of said cross point switch coupled to said input/output pin of said first programmable logic device onto a second input/output pin of said cross point switch coupled to said input/output pin of said second programmable logic device.